Exhibit

6.1

An 18Mb Serial Flash EEPROM for Solid-State Disk Applications

D.J. Lee, R.A. Cernea, M. Mofidi, S. Mehrotra, E.Y. Chang, W.Y. Chien, L. Goh, J.H. Yuan, A. Mihnea, G. Sumachisa, Y. Fong, D.C. Guterman, and R.D. Norman
SunDisk Corporation, Santa Clara, CA

K. Sato, H. Onishi, K. Ueda, F. Noro, K. Miyamoto, M. Morita, K. Umeda, and K. Kubo
Matsushita Electronic Corporation, Kyoto, JAPAN

INTRODUCTION

High density FLASH EEPROM for solid state disk applications requires minimization of die area while maintaining the flexibility and controllability needed for low cost storage systems. This 18Mb serial FLASH EEPROM utilizes standard 512B sectoring for erase and high parallelism for program and read operations. Erase sector grouping reduces the erase selection circuits by a factor of four over previous designs and a 256 bit programming *chunk* size increases the program data rate by a factor of four while a *shared data latch architecture* maintains a similar cell size versus sense area pitch compared to previous designs [1]. In addition, a serial chip selection scheme[1] which requires minimal die area enables multiple chip operations to be easily performed.

The die is fabricated using a triple poly, single metal, twin well 0.5u CMOS process with memory cell size of $2.1u^2$ and die size of 396 mils X 290 mils (74 mm^2). The split gate, buried n+ source/drain, virtual ground Flash EEPROM memory uses channel hot electron injection for programming and inter poly dielectric tunneling for erase (see figure 1 for cell operation voltages).

SERIAL INTERFACE / CHIP SELECTION

This serial access memory chip[1] is designed to be used in multi-chip systems and uses a dedicated PCMCIA ATA type II controller. A block diagram of the storage system is shown in figure 2. The serial interface, read protocol, sensing circuits and register architecture have been previously described [1]. Program and erase voltages, timing and error correction (ecc) are controlled externally. In the system, each chip's six address pins are decoded (hard wired to ground and/or VDD) to indicate an individual chip select code identity. To serially select a chip, the *CS* pin is taken high; *PD* acts as the clock signal, and data input to SI(0:1) for all chips is used to compare with each chips identity code. On the falling edge of *CS*, the input code is latched and compared with all chip's identity codes. If a match occurs, that chip is selected and is enabled to receive other commands. Multiple chip select lines are unnecessary; system routing is minimized and chip packing density maximized. Several chips may be sequentially selected in this way so that operations can be broadcast in parallel to multiple chips in a system.[1]

GLOBAL ARCHITECTURE

The 18Mb flash memory device is organized into four quadrants, each with 2304 columns and 2048 rows (see figure 3). One quadrant contains 1024, two-row sectors comprised of 512 bytes for user data, and 64 bytes for overhead and error correction information (ECC). Each row is further divided into nine, 256 bit *chunks* used as the smallest increment for *program* or *read* operations; the 576 byte sector is the smallest unit for *erase* operations. The programming of 256 bits simultaneously is made possible by a low programming current cell design.

Each row-pair shares one common erase gate word line. New to this design is an additional erase pump (ep) decode which enables one erase gate pump to be used for four sectors (see figure 4). The *ep* lines are latch-gated pumped signals which further decode a one of four selection of sectors to be erased. In this way, the pitch of the erase gate pumps and erase gate selection latches (tag-latches) are reduced to 1/4 the area of previous designs while maintaining full and discrete selection of individual (or multiple, if desired) sector erase (typical 1ms pulse).

The 256 bit chunk is programmed or read through the parallel upload or download from an adjacent data register. During programming, bit lines (256 bits) are selectively brought to their programming level after serially loading the data into the data register. During READ, the simultaneous sensing of the 256 bits' cell currents is used to set or reset the data register latches which is then serially shifted to the output while the next chunk is being accessed. The data register is physically separated so that half of each register is on either the top or bottom of each quadrant. This doubles the effective layout pitch of the register and allows the center registers to be shared by the top and bottom quadrants.

CHUNK PROGRAM AND BIT LINE REGULATION

During programming, the bit lines are regulated[1] as a function of a controller supplied voltage source. This eliminates bit line voltage cell load current dependence and ensures more consistent programming (typical 5us pulse) characteristics and resistance to disturbs resultant from voltage spikes. Figure 5 shows the circuit diagram of the bit line regulation circuit and data latch. Vbl is an internally buffered version of the external voltage supply. Transistors M1 through M9 represent one side of a differential amplifier. Vbl is incident to M10 which is the other side of the differential amplifier. M11 and M12 are transistors in an active load configuration and M13 is a current mirrored transistor to a regulated current source. The circuit is repeated for each sense block (256 times) and is gated to a selected bit line with a traditional Y select decode. The data latch portion of the circuit consists of inverters I1 though I4 and transfer gates T1 and T2. Transistor M15 is the program load which pulls the associated data line to the bit line voltage dependent on the state

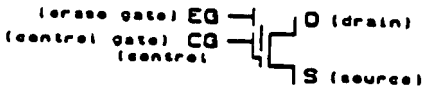
[1] US Patents pending [2] US Patent #5,172,338

0-7803-1918-4/94/$3.00

of I3 and I4 through transistor M16. M17 is the reset transistor which resets the data latch.

REFERENCE CELL ARCHITECTURE

Figure 6 shows the reference cell block. At factory test, the flash EEPROM reference cell current is compared to an externally supplied current so that subsequent programming and erasing of the reference cell can be used to precisely set its desired value (e.g., 1/2 the normal read current) for subsequent field applications.[2] This adjustable reference cell provides an easy means to optimize performance and reliability characteristics of the memory. Transistor C1 is the reference cell which is programmed through m0, m1 and m2 with gate voltage, Vg and drain voltage, Vbl. Vb sets the *drain bias* through m3 and the current is mirrored via m5 through m8 creating Cref which is routed to the 256 sense amplifiers to compare with the selected cells. For reference cell read, current is input through SI(0), mirrored through m10 and compared to Cref by m11 and m12. The output of the comparison is routed to the output buffers.



	CG	EG	D	S
Program	10V	0V	7V	0V
Erase	0V	10V to 22V	0V	0V
Read	5V	0V	1.2V	0V

Figure 1: Cell Operation Voltages

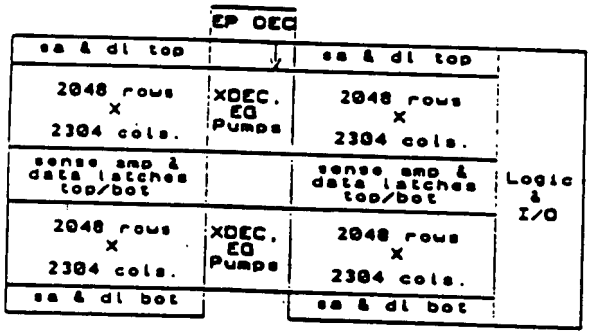


Figure 3: Chip Architecture

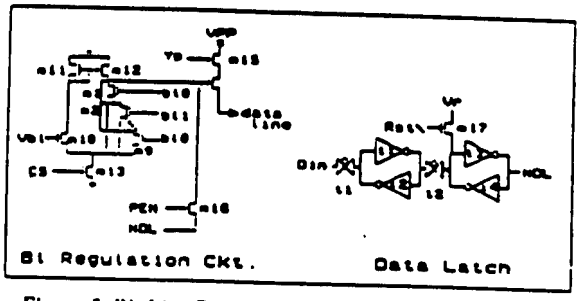


Figure 5: Bit Line Regulation and Data Latch Circuits

CONCLUSION

A low cost high density 18Mb serial FLASH EEPROM for solid state disk applications has been described. Utilizing an improved architecture, higher performance and a smaller die size is achieved while maintaining a small sector size and flexibility for use with its dedicated controller for improved endurance and high reliability.

ACKNOWLEDGMENTS

The authors would like to thank Dr. H. Iwasa, Dr. T. Kawasaki, Mr. Y. Furuta, Mr. H. Sato, Mr. T. Ogawa, Mr. T. Kazumi, Mr. A. Yamada, and Mr. S. Chaya from Matsushita Electronic Corporation, Mr. B. Bortfeld, Mr. D. Auclair, and Dr. E. Harari, from SunDisk Corporation, for their support of this project. The authors would also like to thank B. Kawaguchi, and F. Santos for CAD support.

REFERENCE

[1] Mehrotra, et al., "Serial 9Mb Flash EEPROM for Solid State Disk Applications," 1992 Symposium on VLSI Dig. of Tech Papers

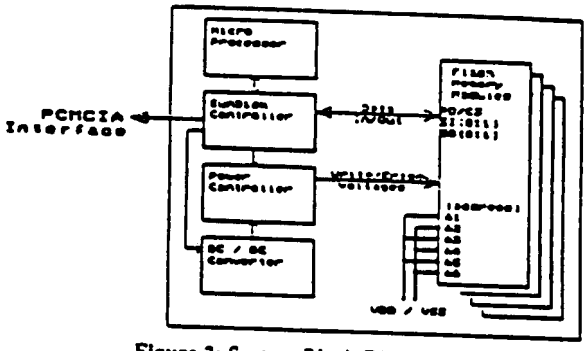


Figure 2: System Block Diagram

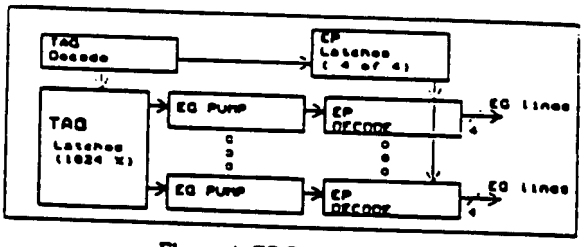


Figure 4: EP Decode Detail

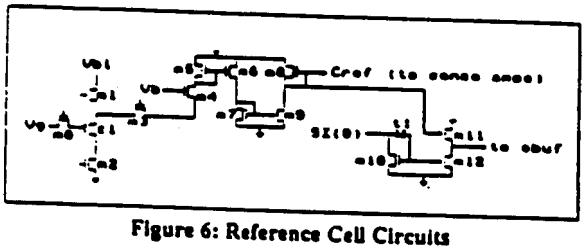


Figure 6: Reference Cell Circuits